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1 **Performance analysis of MAP decoded space-time orthogonal block codes for non-uniform sources**
Behnamfar, F.; Alajaji, F.; Linder, T.;
Information Theory Workshop, 2003. Proceedings. 2003 IEEE , 31 March-4 Ap
2003
Pages:46 - 49

[Abstract]   [PDF Full-Text (444 KB)]   **IEEE CNF**

2 **BEM-based SISO detection of space-time block coded signals transn over frequency-flat fading channels**
Chiavaccini, E.; Gallo, A.S.; Muratori, F.; Vitetta, G.M.;
Global Telecommunications Conference, 2002. GLOBECOM '02. IEEE , Volume
1 , 17-21 Nov. 2002
Pages:374 - 378 vol.1

[Abstract]   [PDF Full-Text (333 KB)]   **IEEE CNF**

3 **Concatenation of space-time block codes and "turbo"-TCM**
Bauch, G.;
Communications, 1999. ICC '99. 1999 IEEE International Conference on , Volu
2 , 6-10 June 1999
Pages:1202 - 1206 vol.2

[Abstract]   [PDF Full-Text (476 KB)]   **IEEE CNF**

4 **Space frequency block coded turbo-BLAST detection for MIMO-OFDN systems**
Sohn, I.;
Electronics Letters , Volume: 39 , Issue: 21 , 16 Oct. 2003

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Pages:1557 - 1558

[Abstract]   [PDF Full-Text (214 KB)]   **IEE JNL**

5 Channel estimation for space-time block coded OFDM systems in the presence of multipath fading

Panayirci, E.; Cirpan, H.A.;
Global Telecommunications Conference, 2002. GLOBECOM '02. IEEE , Volume 2 , 17-21 Nov. 2002
Pages:1157 - 1161 vol.2

[Abstract]   [PDF Full-Text (392 KB)]   **IEEE CNF**

6 BEM-Based SISO Detection of Orthogonal Space–Time Block Codes (Frequency Flat-Fading Channels

Gallo, A.S.; Chiavaccini, E.; Muratori, F.; Vitetta, G.M.;
Wireless Communications, IEEE Transactions on , Volume: 3 , Issue: 6 , Nov.

Pages:1885 - 1889

[Abstract]   [PDF Full-Text (208 KB)]   **IEEE JNL**

7 Multispectral image fusion using local mapping techniques

Scheunders, P.;
Pattern Recognition, 2000. Proceedings. 15th International Conference on , Volume: 2 , 3-7 Sept 2000
Pages:311 - 314 vol.2

[Abstract]   [PDF Full-Text (752 KB)]   **IEEE CNF**

8 Bayesian Monte Carlo multiuser receiver for space-time coded multicarrier CDMA systems

Zigang Yang; Ben Lu; Xiaodong Wang;
Selected Areas in Communications, IEEE Journal on , Volume: 19 , Issue: 8 , . 2001
Pages:1625 - 1637

[Abstract]   [PDF Full-Text (304 KB)]   **IEEE JNL**

9 Iterative receivers for multiuser space-time coding systems

Ben Lu; Xiaodong Wang;
Selected Areas in Communications, IEEE Journal on , Volume: 18 , Issue: 11 , 2000
Pages:2322 - 2335

[Abstract]   [PDF Full-Text (352 KB)]   **IEEE JNL**

10 Decentralized overlapping control of a platoon of vehicles

Stankovic, S.S.; Stanojevic, M.J.; Siljak, D.D.;
Control Systems Technology, IEEE Transactions on , Volume: 8 , Issue: 5 , Se 2000
Pages:816 - 832

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[Abstract]   [PDF Full-Text (396 KB)]   **IEEE JNL**

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11 Binary decoding of concatenated turbo codes and space-time block codes for quaternary modulations
Page, E.C.;
Electrotechnical Conference, 2004. MELECON 2004. Proceedings of the 12th II
Mediterranean , Volume: 3 , 12-15 May 2004
Pages:1159 - 1164 Vol.3

[Abstract]   [PDF Full-Text (584 KB)]   **IEEE CNF**

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12 Joint channel estimation and symbol detection for SFBC-OFDM syst via the EM algorithm
Bing Han; Xiqi Gao; Xiaohu You; Weckerle, M.;
Communications, 2004 IEEE International Conference on , Volume: 6 , 20-24
2004
Pages:3148 - 3152 Vol.6

[Abstract]   [PDF Full-Text (405 KB)]   **IEEE CNF**

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13 A multiuser space-time block coding system with squaring method
Yinggang Du; Chan, K.T.;
Neural Networks and Signal Processing, 2003. Proceedings of the 2003
International Conference on , Volume: 2 , 14-17 Dec. 2003
Pages:1450 - 1454 Vol.2

[Abstract]   [PDF Full-Text (365 KB)]   **IEEE CNF**

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14 Space-time bit-interleaved coded modulation over frequency select fading channels with iterative decoding
Tonello, A.M.;
Global Telecommunications Conference, 2000. GLOBECOM '00. IEEE , Volume
3 , 27 Nov.-1 Dec. 2000
Pages:1616 - 1620 vol.3

[Abstract]   [PDF Full-Text (512 KB)]   **IEEE CNF**

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15 Iterative receivers for multiuser space-time coding systems
Ben Lu; Xiaodong Wang;
Communications, 2000. ICC 2000. 2000 IEEE International Conference
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Pages:302 - 306 vol.1

[Abstract]   [PDF Full-Text (464 KB)]   **IEEE CNF**

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1 Rendering and simulation: Low latency photon mapping using block hashing   ▨
Vincent C. H. Ma, Michael D. McCool
September 2002 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS conference on Graphics hardware**

Full text available: 📄 pdf(3.10 MB)   Additional Information: full citation, abstract, references, citings, index terms

For hardware accelerated rendering, photon mapping is especially useful for simulating caustic lighting effects on non-Lambertian surfaces. However, an efficient hardware algorithm for the computation of the k nearest neighbours to a sample point is required.Existing algorithms are often based on recursive spatial subdivision techniques, such askd-trees. However, hardware implementation of a tree-based algorithm would have a high latency, or would require a large cache to avoid this latency on a ...

2 An improved storage management scheme for block structured languages   ▨
Thomas P. Murtagh
July 1991 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 13 Issue 3
Full text available: 📄 pdf(1.86 MB)   Additional Information: full citation, references, index terms, review

Keywords: activation records, call graphs, internal analysis, procedure call overhead

3 Data-centric multi-level blocking   ▨
Induprakas Kodukula, Nawaaz Ahmed, Keshav Pingali
May 1997 **ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 1997 conference on Programming language design and implementation**, Volume 32 Issue 5
Full text available: 📄 pdf(1.75 MB)   Additional Information: full citation, abstract, references, citings, index terms

We present a simple and novel framework for generating blocked codes for high-performance machines with a memory hierarchy. Unlike traditional compiler techniques like tiling, which are based on reasoning about the control flow of programs, our techniques are based on reasoning directly about the flow of data through the memory hierarchy. Our data-centric transformations permit a more direct solution to the problem of enhancing data locality than current control-centric techniques do, and genera ...

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4 HFS: a performance-oriented flexible file system based on building-block compositions ▨
Orran Krieger, Michael Stumm
May 1996 **Proceedings of the fourth workshop on I/O in parallel and distributed
systems: part of the federated computing research conference**
Full text available: 📄 pdf(1.83 MB)   Additional Information: full citation, references, citings, index terms

5 HFS: a performance-oriented flexible file system based on building-block compositions ▨
Orran Krieger, Michael Stumm
August 1997 **ACM Transactions on Computer Systems (TOCS)**, Volume 15 Issue 3

Full text available: 📄 pdf(363.87 KB)   Additional Information: full citation, abstract, references, citings, index
terms, review

The Hurricane File System (HFS) is designed for (potentially large-scale) shared-memory
multiprocessors. Its architecture is based on the principle that, in order to maximize
performance for applications with diverse requirements, a file system must support a wide
variety of file structures, file system policies, and I/O interfaces. Files in HFS are
implemented using simple building blocks composed in potentially complex ways. This
approach yields great flexibility, allowing an application ...

Keywords: customization, data partitioning, data replication, flexibility, parallel computing,
parallel file system

6 A dynamic and efficient representation of building-block layout ▨
W.-M. Dai, M. Sato, E. S. Kuh
October 1987 **Proceedings of the 24th ACM/IEEE conference on Design automation**

Full text available: 📄 pdf(1.02 MB)   Additional Information: full citation, abstract, references, citings, index
terms

Dynamic layout representation is a key problem in developing a building block layout
system. We have unified topological and geometrical representations, and developed
efficient methods to update topological information after geometrical operations. The
experimental results are very promising. This representation is the key for information flow
in BEAR — a new building block layout system being developed at U. C. Berkeley.

7 Space and time efficient execution of parallel irregular computations ▨
Cong Fu, Tao Yang
June 1997 **ACM SIGPLAN Notices , Proceedings of the sixth ACM SIGPLAN symposium
on Principles and practice of parallel programming**, Volume 32 Issue 7
Full text available: 📄 pdf(1.35 MB)   Additional Information: full citation, abstract, references, citings, index
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Solving problems of large sizes is an important goal for parallel machines with multiple CPU
and memory resources. In this paper, issues of efficient execution of overhead-sensitive
parallel irregular computation under memory constraints are addressed. The irregular
parallelism is modeled by task dependence graphs with mixed granularities. The trade-off in
achieving both time and space efficiency is investigated. The main difficulty of designing
efficient run-time system support is caused by the ...

8 Space/time-efficient scheduling and execution of parallel irregular computations ▨
Tao Yang, Cong Fu
November 1998 **ACM Transactions on Programming Languages and Systems (TOPLAS)**,
Volume 20 Issue 6
Full text available: 📄 pdf(374.95 KB)   Additional Information: full citation, abstract, references, citings, index
terms

In this article we investigate the trade-off between time and space efficiency in scheduling and executing parallel irregular computations on distributed-memory machines. We employ acyclic task dependence graphs to model irregular parallelism with mixed granularity, and we use direct remote memory access to support fast communication. We propose new scheduling techniques and a run-time active memory management scheme to improve memory utilization while retaining good time efficiency, and we ...

Keywords: DAG scheduling, direct remote memory access, irregular parallelism, run-time support

9 Texture compression with adaptive block partitions (poster session)
Leonid Levkovich-Maslyuk, Pavel Kalyuzhny, Alexander Zhirkov
October 2000 **Proceedings of the eighth ACM international conference on Multimedia**

Full text available: pdf(300.75 KB)   Additional Information: full citation, abstract, references, citings, index terms

We present image compression method based on block palletizing. Image block is partitioned into four subsets, and each subset is palletized by 2 or 4 colors from the quasioptimal local palette, constructed for the whole block. Index map for the whole block, being the union of index maps for subsets, is thus only 1 or 2 bits deep, while the local palette may consist of 8 or even 16 colors. The local palette has a specific geometrical configuration in RGB color space, determined by only 2 color ...

Keywords: fast rendering, image compression, local palletizing, texture compression

10 Time and space lower bounds for non-blocking implementations (preliminary version)
Prasad Jayanti, King Tan, Sam Toueg
May 1996 **Proceedings of the fifteenth annual ACM symposium on Principles of distributed computing**
Full text available: pdf(901.43 KB)   Additional Information: full citation, references, citings, index terms

11 Program restructuring for block structured languages
Gopa Kumar, C. Thomas Nute
May 1980 **ACM SIGMETRICS Performance Evaluation Review, Proceedings of the 1980 international symposium on Computer performance modelling, measurement and evaluation**, Volume 9 Issue 2
Full text available: pdf(649.40 KB)   Additional Information: full citation, abstract, references, index terms

Prior studies of program restructuring to increase the degree of locality of a program in a paged virtual memory system were restricted to statically allocated codes only. This work develops a restructuring methodology for block structured languages like Algol, with dynamic memory allocation. We subsequently restructure and analyze different classes of programs using this methodology and study the performance gains realized with different restructuring heuristics.

12 Floorplanning and placement: Dynamic global buffer planning optimization based on detail block locating and congestion analysis
Yuchun Ma, Xianlong Hong, Sheqin Dong, Song Chen, Yici Cai, C. K. Cheng, Jun Gu
June 2003 **Proceedings of the 40th conference on Design automation**

Full text available: pdf(205.60 KB)   Additional Information: full citation, abstract, references, citings, index terms

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By dividing the packing area into routing tiles, we can give the budget of the buffer insertion. And the detail locating of the blocks in their rooms can be implemented for each iterations during the annealing process to favor the later buffer planning. The buffer insertion will affect the possible routes as well the congestion of the packing. The congestion estimation in this paper takes the buffer insertion into account. So we devise a buffer planning algorithm to allocate the buffer into tile ...

Keywords: buffer insertion, congestion, floorplanning, routability

13 Contributed articles on online, interactive, and anytime data mining: Mining data streams under block evolution
Venkatesh Ganti, Johannes Gehrke, Raghu Ramakrishnan
January 2002 **ACM SIGKDD Explorations Newsletter**, Volume 3 Issue 2

Full text available: pdf(1.10 MB)   Additional Information: full citation, abstract, references, citings

In this paper we survey recent work on incremental data mining model maintenance and change detection under *block evolution*. In block evolution, a dataset is updated periodically through insertions and deletions of *blocks* of records at a time. We describe two techniques: (1) We describe a generic algorithm for model maintenance that takes any traditional incremental data mining model maintenance algorithm and transforms it into an algorithm that allows restrictions on a temporal su ...

14 Blocking and array contraction across arbitrarily nested loops using affine partitioning
Amy W. Lim, Shih-Wei Liao, Monica S. Lam
June 2001 **ACM SIGPLAN Notices , Proceedings of the eighth ACM SIGPLAN symposium on Principles and practices of parallel programming**, Volume 36 Issue 7

Full text available: pdf(290.60 KB)   Additional Information: full citation, abstract, references, citings, index terms

Applicable to arbitrary sequences and nests of loops, affine partitioning is a program transformation framework that unifies many previously proposed loop transformations, including unimodular transforms, fusion, fission, reindexing, scaling and statement reordering. Algorithms based on affine partitioning have been shown to be effective for parallelization and communication minimization. This paper presents algorithms that improve data locality using affine partitioning.Blockin ...

15 The Quadtree and Related Hierarchical Data Structures
Hanan Samet
June 1984 **ACM Computing Surveys (CSUR)**, Volume 16 Issue 2

Full text available: pdf(4.87 MB)   Additional Information: full citation, references, citings, index terms

16 Data remapping for design space optimization of embedded memory systems
Rodric M. Rabbah, Krishna V. Palem
May 2003 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 2 Issue 2

Full text available: pdf(855.05 KB)   Additional Information: full citation, abstract, references, citings, index terms

In this article, we present a novel linear time algorithm for *data remapping*, that is, (i) lightweight; (ii) fully automated; and (iii) applicable in the context of pointer-centric programming languages with dynamic memory allocation support. All previous work in this area lacks one or more of these features. We proceed to demonstrate a *novel application of this algorithm as a key step in optimizing the design of an embedded memory system.* Specifically, we show that by virtue of lo ...

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Keywords: Design space exploration, caches, compiler optimization, data remapping, embedded systems, memory hierarchy, memory subsystem

17 Special Section on Science of Network Design: Building the blocks of protocol design and analysis: challenges and lessons learned from case studies on mobile ad hoc routing and micro-mobility protocols
Fan Bai, Ganesha Bhaskara, Ahmed Helmy
July 2004 **ACM SIGCOMM Computer Communication Review**, Volume 34 Issue 3

Full text available: pdf(573.77 KB)   Additional Information: full citation, abstract, references, index terms

With the emergence of new application-specific sensor and Ad-hoc networks, increasingly complex and custom protocols will be designed and deployed. We propose a framework to systematically design and evaluate networking protocols based on a 'building block' approach. In this approach, each protocol is broken down into a set of parameterized modules called "building blocks", each having its own specific functionality. The properties of these building blocks and their interaction define the ove ...

Keywords: building block, micro-mobility, mobile ad hoc network, protocol analysis, protocol design

18 Exact analysis of the cache behavior of nested loops
Siddhartha Chatterjee, Erin Parker, Philip J. Hanlon, Alvin R. Lebeck
May 2001 **ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 2001 conference on Programming language design and implementation**, Volume 36 Issue 5

Full text available: pdf(1.66 MB)   Additional Information: full citation, abstract, references, citings, index terms

We develop from first principles an exact model of the behavior of loop nests executing in a memory hierarchy, by using a nontraditional classification of misses that has the key property of composability. We use Presburger formulas to express various kinds of misses as well as the state of the cache at the end of the loop nest. We use existing tools to simplify these formulas and to count cache misses. The model is powerful enough to handle imperfect loop nests and various flavors of non-lin ...

19 Third Generation Computer Systems
Peter J. Denning
December 1971 **ACM Computing Surveys (CSUR)**, Volume 3 Issue 4

Full text available: pdf(3.52 MB)   Additional Information: full citation, abstract, references, citings, index terms

The common features of third generation operating systems are surveyed from a general view, with emphasis on the common abstractions that constitute at least the basis for a "theory" of operating systems. Properties of specific systems are not discussed except where examples are useful. The technical aspects of issues and concepts are stressed, the nontechnical aspects mentioned only briefly. A perfunctory knowledge of third generation systems is presumed.

20 A declarative approach to optimize bulk loading into databases
Sihem Amer-Yahia, Sophie Cluet
June 2004 **ACM Transactions on Database Systems (TODS)**, Volume 29 Issue 2

Full text available: pdf(1.00 MB)   Additional Information: full citation, abstract, references, index terms

Applications, such as warehouse maintenance, need to load large data volumes regularly.

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The efficiency of loading depends on the resources that are available at the source and at the target systems. Our work aims to understand the performance criteria that are involved in bulk loading data into a database and to devise tailored optimization strategies.Unlike commercial systems and previous research on the same topic, our approach follows the fundamental database principle of physical-logical ind ...

Keywords: Declarative bulk loading, algebra, recovery, side-effects

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